What is claimed is:

1. A method for reducing signal distortion in a receiver, comprising:

deriving a sequence of chips from a received signal;

canceling postcursor-ISI from the chip sequence to produce a chip metric;

determining a current CCK codeword based on said chip metric;

computing a chip-time reversed estimate of the current CCK codeword; and

canceling precursor-ISI from a previous CCK codeword based on the chip-time reversed estimate of the current CCK codeword.

2. The method of claim 1, wherein deriving the chip sequence includes:

convolving the received signal with coefficients of a channel matched filter.

3. The method of claim 1, further comprising:

generating terms for canceling the postcursor ISI from a chip sequence detected in a preceding symbol.

4. The method of claim 1, wherein canceling postcursor-ISI includes:

generating postcursor-ISI cancellation terms from a previously detected CCK chip sequence used to form a previous CCK codeword; and

subtracting the postcurstor-ISI cancellation terms from the chip sequence to produce said chip metric.

5. The method of claim 1, wherein canceling postcursor-ISI includes:

setting DFE coefficients based on a previously detected CCK chip sequence;

generating postcursor-ISI terms by shifting the DFE coefficients a predetermined number of times per chip clock;

subtracting the postcursor-ISI terms from the chip sequence to produce said chip metric.

6. The method of claim 1, wherein the current CCK codeword is generated by inputting said chip metric into a CCK correlator.

7. The method of claim 1, wherein canceling the precursor-ISI includes:

computing conjugates of chip values of a future symbol;

setting DFE coefficients based on the conjugates;

generating precursor-ISI terms by shifting the DFE coefficients a predetermined number of times per chip clock; and

subtracting the precursor-ISI terms from chip metrics corresponding to the previous CCK codeword.

8. The method of claim 1, wherein the received signal is one generated in a DSSS/CCK wireless communications system.

9. The method of claim 1, further comprising:

equalizing signal energy in a codeword correlator bank used to generate the current and previous CCK codewords.

10. The method of claim 1, further comprising:

(a) obtaining chips of the previous CCK codeword generated after cancellation of the precursor-ISI; and

(b) performing postcursor-ISI and precursor-ISI based on the previous CCK codeword chips obtained in (a).

11. The method of claim 10, further comprising:

repeating steps (a) and (b) a predetermined number of times.

12. A system for reducing signal distortion in a receiver, comprising:

channel matched filter which generates a sequence of chips from a received signal;

a decision feedback equalizer (DFE) which cancels postcursor-ISI from the chip sequence to produce a chip metric; and

a CCK correlation-decision block which generates a current CCK codeword based on said chip metric, wherein the DFE cancels precursor-ISI from a previous CCK codeword based on a chip-time reversed estimate of the current CCK codeword.

13. The method of claim 12, wherein the DFE cancels postcursor-ISI by generating postcursor-ISI correction terms from a previously detected CCK chip sequence used to form the previous CCK codeword and subtracting the postcurstor-ISI correction terms from the chip sequence to produce said chip metric.

14. The system of claim 12, wherein the DFE cancels postcursor-ISI by setting DFE coefficients based on a previously detected CCK chip sequence, generating postcursor-ISI terms by shifting the DFE coefficients a predetermined number of times per chip clock, and subtracting the postcursor-ISI terms from the chip sequence to produce said chip metric to produce said chip.

15. The system of claim 12, wherein the DFE cancels the precursor-ISI by computing conjugates of chip values of a future symbol, setting DFE coefficients based on the conjugates, generating precursor-ISI terms by shifting the DFE coefficients a predetermined number of times per chip clock, and subtracting the precursor-ISI terms from chip metrics corresponding to the previous CCK codeword.

16. The system of claim 12, wherein the receiver is a DSSS/CCK wireless communications receiver.

17. The system of claim 12, further comprising:

an energy bias canceler which equalizes signal energy in the codeword correlator bank.

18. A bidirectional turbo ISI canceler (BTIC), comprising:

a single-symbol detector which generates a sequence of chips from a received signal;

a postcursor-ISI canceler which cancels postcursor-ISI from the chip sequence to produce a chip metric; and

a precursor-ISI canceler which cancels precursor-ISI based on a chip-time reversed estimate of a current CCK codeword generated from said chip metric.

19. The bidirectional turbo ISI canceler of claim 18, wherein the single-symbol detector includes a RAKE receiver.

20. The bidirectional turbo ISI canceler of claim 18, wherein the single-symbol detector includes:

a channel matched filter which generates the chip sequence from the received signal; and

a codeword correlator bank which generates the current CCK codeword from said chip metric.

21. The bidirectional turbo ISI canceler of claim 20, wherein the single-symbol detector futher includes an energy bias canceler to equalize signal energy in the codeword correlator bank.

22. A method for reducing distortion in a receiver, comprising:

computing a set of DFE coefficients;

canceling postcursor-ISI caused by a preceding symbol using the set of DFE coefficients; and

canceling precursor-ISI caused by a trailing symbol using the same set of DFE coefficients.

23. A receiver, comprising:

a first canceler which cancels postcursor-ISI caused by a preceding symbol;

a second canceler which cancels precursor-ISI caused by a trailing symbol, wherein the first and second cancellers use a same set of DFE coefficients to cancel the postcursor-ISI and precursor-ISI.

24. The receiver of claim 23, wherein the first and second cancellers are included in a same DFE.